Docket No.: 50090-240

UTILITY PATENT APPLICATION UNDER 37 CFR 1.53(b)

Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231
Sir:

Transmitted herewith for filing is the patent application of:

INVENTOR: Kazuyuki NAKAGAWA, Michitaka KIMURA, Masatoshi YASUNAGA
FOR: SEMICONDUCTOR DEVICE HAVING AN IMPROVED MOUNTING STRUCTURE

Enclosed are:

- ☒ 14 pages of specification, claims, abstract.
- ☒ Declaration and Power of Attorney.
- ☒ Priority Claimed.
- ☒ Certified copy of Japanese Patent Application No. 2000-081026
- ☒ 3 sheets of formal drawing.
- ☒ An assignment of the invention to Mitsubishi Denki Kabushiki Kaisha and the assignment recordation fee.
- ☐ An associate power of attorney.
- ☐ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27.
- ☐ Information Disclosure Statement, Form PTO-1449 and reference.
- ☒ Return Receipt Postcard
- ☐

The filing fee has been calculated as shown below:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	3	-20	0	$18.00	$0.00
Independent Claims	1	-3	0	$78.00	$0.00
				Multiple Dependent Claim(s)	$0.00
				Basic Fee	$690.00
				Total of Above Calculations	$690.00
				Less ½ for Small Entity	$0.00
				Assignment & Recording Fee	$40.00
				Total Fee	$730.00

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Respectfully submitted,

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SEMICONDUCTOR DEVICE HAVING AN IMPROVED MOUNTING STRUCTURE

Background of the Invention

Field of the Invention

The present invention relates to a semiconductor device in which a semiconductor element is mounted to an insulating circuit board, and more particularly, to a semiconductor device whose reliability of mounting is improved by means of improving a joint between a semiconductor element and an insulating circuit board, to thereby alleviate stress developing in a solder joint formed on each of external electrodes of the semiconductor device.

Background Art

FIG. 4 is a cross-sectional view showing a conventional semiconductor device in which a semiconductor element is mounted on the insulating circuit board.

As shown in FIG. 4, in the conventional semiconductor device, a semiconductor element 10 is mounted face-down on a circuit board 1 through use of an adhesive layer 5. An element electrode 11 is connected to a board electrode 4 provided on the lower surface of the circuit board 1 via an opening hole 2 formed therein and through use of a wire 12. The joint between the element electrode 11 and the board electrode 4 is sealed with resin 6. External electrodes 3 are provided on the lower surface of the circuit board 1. Each of the external electrodes 3 is fixedly mounted on the circuit board 1 via a solder joint 31 and on a module board 200 via a solder joint 32.

While the semiconductor element 10 is placed face-down on the insulating circuit board 1, the semiconductor element electrode 11 and a board electrode 4 provided on the lower surface of the insulating circuit board 1 are electrically interconnected by way of the opening hole 2 of the insulating circuit board 1. In the semiconductor device

in which the joint between the semiconductor element electrode 11 and the board electrode 4 is sealed with resin, an adhesive layer 5 for bonding together the semiconductor element 10 and the insulating circuit board 1 is equal in size with the semiconductor element 10.

The semiconductor device 100 having such a configuration is fixedly mounted on the module board 200 via the external electrodes 3.

FIG. 5 is a cross-sectional view showing another conventional semiconductor device. The semiconductor device shown in FIG. 5 corresponds to the semiconductor device 100 shown in FIG. 4, in which the surrounding regions of the side surfaces of the semiconductor element 10 are additionally coated with sealing resin 7 so as to assume a flange structure. More specifically, the semiconductor device corresponds to the conventional semiconductor device shown in FIG. 4, in which the side surfaces of the semiconductor element 10 are sealed with resin so as to assume a flange structure.

In the conventional semiconductor devices shown in FIGS. 4 and 5, the resin of the adhesive layer 5 used for bonding the semiconductor element 10 to the insulating circuit board 1 is substantially equal in size with the semiconductor element 10. Stress due to a difference in thermal expansion coefficients of the constituent members of the semiconductor device 100 is exerted on the external electrodes 3 provided on the outermost periphery of the insulating circuit board 1, thereby resulting in a tendency toward a reduction in the reliability of packaging of the semiconductor device 100.

Further, there has recently been posed the task of prolonging the life of solder joints in a temperature cycle test, where a semiconductor device is mounted on a module board.

The present invention has been conceived to solve such a problem in the background art and is aimed at providing a semiconductor device which has improved joints between an insulating circuit board and a semiconductor element and improved reliability of mounting and which

attains prolonged life of solder joints in a temperature cycle test to which the semiconductor device is subjected while being mounted on the module board.

Summary of the Invention

According to one aspect of the present invention, a semiconductor device comprises a semiconductor element bonded to a circuit board. The semiconductor element has a primary surface and a back surface, and has an element electrode on the primary surface. The circuit board has a primary surface and a back surface, and has a board electrode on at least the back surface. The circuit board has a predetermined opening hole formed therein. The primary surface of the semiconductor element is bonded to the primary surface of the circuit board by means of an adhesive layer which is greater in size than the primary surface of the semiconductor element, and the element electrode of the semiconductor element is connected to the board electrode provided on the back surface of the circuit board via the opening hole.

Other and further objects, features and advantages of the invention will appear more fully from the following description.

Brief Description of the Drawings

FIG. 1 is a cross-sectional view showing a semiconductor device according to a first embodiment of the present invention, in which a semiconductor element is placed face-down on an insulating circuit board, and the semiconductor device is mounted on a module board.

FIG. 2 is a cross-sectional view showing a semiconductor device according to a second embodiment of the present invention, in which a semiconductor element is bonded face-down to the insulating circuit board, and the semiconductor device is mounted on a module board.

FIG. 3 is a cross-sectional view showing a semiconductor device according to a third embodiment of the present invention, in which a semiconductor element is bonded face-down to the insulating circuit

board, and the semiconductor device is mounted on a module board.

FIG. 4 is a cross-sectional view showing a conventional semiconductor device in which a semiconductor element is mounted on the insulating circuit board, and the semiconductor device is mounted on a module board.

FIG. 5 is a cross-sectional view showing another conventional semiconductor device.

Detailed Description of the Preferred Embodiments

Preferred embodiments of the present invention will now be described by reference to the accompanying drawings. Throughout the drawings, like reference numerals designate like or corresponding elements, and repetition of their explanations is omitted here for brevity, as required.

First Embodiment

FIG. 1 is a cross-sectional view showing a semiconductor device according to a first embodiment of the present invention, in which a semiconductor element is placed face-down on an insulating circuit board, and the semiconductor device is mounted on a module board. In the first embodiment, an adhesive layer for bonding the semiconductor element to the insulating circuit board is greater in size than the semiconductor element.

In FIG. 1, reference numeral 1 designates an insulating circuit board for bonding a semiconductor element; 2 designates an opening hole formed in the insulating circuit board 1 for passage of an interconnection pattern; 3 designates an external electrode of the insulating circuit board 1; and 4 designates a board electrode (i.e., a lower-surface board electrode) provided on the lower surface of the insulating circuit board 1.

Reference numeral 10 designates a semiconductor element bonded face-down to the circuit board 1; 11 designates an element electrode of the semiconductor element 10; and 12 designates a wire for

electrically connecting the element electrode 11 to the lower-surface board electrode 4.

Reference numeral 5a designates an adhesive layer which is formed so as to become larger than the semiconductor element 10 and fixedly bonds the semiconductor element 10 to the circuit board 1; and 6 designates sealing resin for sealing a portion of the semiconductor element 10 and the wire 12 which is exposed on the lower surface of the circuit board 1.

The opening hole 2 is formed in the insulating circuit board 1, and the semiconductor element 10 is bonded face-down to the insulating circuit board 1 by means of the adhesive layer 5a which extends so as to become larger than the semiconductor element 10. The semiconductor element electrode 11 is electrically connected to the lower-surface board electrode 4 via the opening hole 2 of the insulating circuit board 1.

Reference numeral 100A designates a semiconductor device having the foregoing configuration.

Reference numeral 200 designates a module board, and the semiconductor device 100 is mounted on the module board 200 via the external electrodes 3. The external electrodes 3 are formed from solder balls. The insulating circuit board 1 is bonded to each external electrode 3 via a solder joint 31, and the respective external electrode 3 is bonded to the module board 200 via a solder joint 32.

The semiconductor device 100A having such a structure is subjected to a temperature cycle test while being mounted on the module board 200. As a result, there are alleviated the stress imposed on the solder joint 31 between the respective external electrode 3 and the insulating circuit board 1 and the stress imposed on the solder joint 32 between the respective external electrode 3 and the module board 200.

This phenomenon can be explained as follows. In the conventional semiconductor device shown in FIG. 4, stress due to a difference between

coefficients of thermal expansion of constituent members of the semiconductor device 100 is exerted on the external electrode 3 provided on the outermost periphery of the semiconductor device 100, thereby deteriorating the reliability of packaging of the semiconductor device 100. In contrast, in the structure of the semiconductor device 100A according to the present embodiment, the area covered by the adhesive layer 5a for absorbing the stress due to a difference in thermal expansion coefficients is greater than the semiconductor element 10. Accordingly, the stress exerted on the solder joints 31 and 32 is alleviated, thus improving the reliability of packaging of the semiconductor device 100A.

The structure of the semiconductor device according to the first embodiment may be summarized as follows. The circuit board 1 has a primary surface and a back surface, and the predetermined opening hole 2 is formed in the circuit board 1. The board electrode 4 is provided on at least the back surface of the circuit board 1. The semiconductor element 10 has a primary surface and a back surface, and the element electrode 11 is placed on the primary surface of the semiconductor element 10. The primary surface of the semiconductor element 10 is bonded to the primary surface of the circuit board 1 by means of the adhesive layer 5a, which is greater in size than the primary surface of the semiconductor element 10. The element electrode 11 of the semiconductor element 10 is connected to the board electrode 4 provided on the back surface of the circuit board 1, via the opening hole 2 formed therein.

More specifically, the adhesive layer 5a is greater in size than the semiconductor element 10 such that the entirety of the primary surface of the semiconductor element 10 is covered by the adhesive layer 5a and the adhesive layer 5a extends to the outside of the semiconductor element 10 to a predetermined distance.

Second Embodiment

FIG. 2 is a cross-sectional view showing a semiconductor device according to a second embodiment of the present invention, in which a semiconductor element is bonded face-down to the insulating circuit board, and the semiconductor device is mounted on a module board. In the second embodiment, the semiconductor device comprises the semiconductor element whose side surfaces are sealed with resin so as to assume a flange structure. Further, an adhesive layer for bonding the semiconductor element to the insulating circuit board is greater in size than the semiconductor element.

In FIG. 2, reference numeral 1 designates a circuit board; 2 designates an opening hole of the circuit board 1; 3 designates an external electrode of the circuit board 1; and 4 designates a lower-surface board electrode provided on the lower surface of the circuit board 1. Further, reference numeral 10 designates a semiconductor element; 11 designates an element electrode of the semiconductor element 10; and 12 designates a wire for electrically connecting the element electrode 11 to the lower-surface board electrode 4.

Reference numeral 5a designates an adhesive layer which is greater in size than the semiconductor element 10; and 6 designates sealing resin. Reference numeral 7a designates resin for sealing surrounding regions of the side surfaces of the semiconductor element 10 so as to assume a flange structure.

As mentioned above, the opening hole 2 is formed in the circuit board 1, and the semiconductor element 10 is bonded face-down to the circuit board 1 by means of the adhesive layer 5a which extends so as to become greater in size than the semiconductor element 10. The semiconductor element electrode 11 is electrically connected to the lower-surface board electrode 4 via the opening hole 2 of the circuit board 1. Surrounding regions of the side surfaces of the semiconductor element 10 are sealed with the resin 7a, to thereby assume a flange

structure. Reference numeral 100B designates a semiconductor device having the foregoing structure.

Reference numeral 200 designates a module board, and the semiconductor device 100B is mounted on the module board 200 via the external electrodes 3. The external electrodes 3 are formed from solder balls. The insulating circuit board 1 is bonded to each external electrode 3 via a solder joint 31, and the respective external electrode 3 is bonded to the module board 200 via a solder joint 32.

The semiconductor device 100B having such a structure is subjected to a temperature cycle test while being mounted on the module board 200. As a result, there are alleviated the stress imposed on the solder joint 31 between the respective external electrode 3 and the insulating circuit board 1 and the stress imposed on the solder joint 32 between the respective external electrode 3 and the module board 200.

The reason for this is as follows. In the conventional semiconductor device shown in FIG. 5, the circuit board 1 becomes warped about a point in the vicinity of the edge of the semiconductor element 10, thereby shortening the life of solder joints of the semiconductor device 100. As shown in the present embodiment, since the adhesive layer 5a is made larger than the semiconductor element 10, the point about which the circuit board 1 is to warp is distant from the external electrodes 3 provided on the outermost periphery of the semiconductor device 100B. As a result, the stress exerted on the solder joints 31 and 32 of the respective external electrode 3 is alleviated, thereby improving the reliability of packaging of the semiconductor device 100B. As mentioned above, in the present embodiment, the rigidity and reliability of packaging of the semiconductor device 100B are improved.

Third Embodiment

FIG. 3 is a cross-sectional view showing a semiconductor device according to a third embodiment of the present invention, in which a

semiconductor element is bonded face-down to the insulating circuit board, and the semiconductor device is mounted on a module board. In the third embodiment, the side surfaces and back surface of the semiconductor element are sealed with resin assuming a flange structure in the periphery. Further, an adhesive layer for bonding the semiconductor element to the insulating circuit board is larger in size than the semiconductor element.

In FIG. 3, reference numeral 1 designates a circuit board; 2 designates an opening hole formed in the circuit board 1; 3 designates an external electrode of the circuit board 1; and 4 designates lower-surface electrodes of the circuit board 1. Further, reference numeral 10 designates a semiconductor element; 11 designates an element electrode of the semiconductor element 10; and 12 designates a wire for electrically connecting the element electrode 11 to the lower-surface board electrode 4.

Reference numeral 5a designates an adhesive layer which is larger in size than the semiconductor element 10 and bonds the semiconductor element 10 to the circuit board 1; and 6 designates sealing resin.

Reference numeral 7b designates resin for sealing surrounding regions of the side surfaces and back surface of the semiconductor element 10 (here the back surface corresponds to a surface opposite the surface of the semiconductor element 10 having the element electrode 11 mounted thereon), and the resin 7a assumes a flange structure in its periphery.

As mentioned above, in the present embodiment, the opening hole 2 is formed in the circuit board 1, and the semiconductor element 10 is bonded face-down to the circuit board 1 by means of the adhesive layer 5a which extends to the larger size than the semiconductor element 10. The semiconductor element electrode 11 is electrically connected to the lower-surface board electrode 4 via the opening hole 2 of the circuit board 1. Surrounding regions of the side surfaces and back surface of the semiconductor element 10 are sealed with the resin 7b,

and the portion of the resin 7b which seals surrounding regions of the side surfaces of the semiconductor element 10 assumes a flange structure. The sealing resin 7b corresponds to the sealing resin 7a of flange structure shown in FIG. 2, in a case where a resin layer of predetermined thickness is additionally and integrally formed from the sealing resin 7a onto the back surface of the semiconductor element 11. Reference numeral 100C designates a semiconductor device having the foregoing structure.

Reference numeral 200 designates a module board, and the semiconductor device 100C is mounted on the module board 200 via the external electrodes 3. The external electrodes 3 are formed from solder balls. The insulating circuit board 1 is bonded to each external electrode 3 via a solder joint 31, and the respective external electrode 3 is bonded to the module board 200 via a solder joint 32.

The semiconductor device 100C having such a structure is subjected to a temperature cycle test while being mounted on the module board 200. As a result, there are alleviated the stress imposed on the solder joint 31 between the respective external electrode 3 and the insulating circuit board 1 and the stress imposed on the solder joint 32 between the respective external electrode 3 and the module board 200.

The reason for this is as follows. In the conventional semiconductor device shown in FIG. 5, the circuit board 1 becomes warped about a point in the vicinity of the edge of the semiconductor element 10, thereby shortening the life of solder joints of the semiconductor device 100. In the case of the semiconductor device 100C according to the present embodiment, since the adhesive layer 5a is made so as to become larger in size than the semiconductor element 10, the point about which the circuit board 1 is to warp is distant from the external electrodes 3 provided on the outermost periphery of the semiconductor device 100C. As a result, the stress exerted on the solder joints 31 and 32 of the respective external electrode 3 is alleviated, thereby

improving the reliability of packaging of the semiconductor device 100C.

Further, the sealing resin 7b assuming a flange structure is bonded to the circuit board 1 via the adhesive layer 5a having a high bonding characteristic. As a result, there can be prevented a decrease in the reliability of packaging of the semiconductor device 100C, which would otherwise be caused when the circuit board 1 is exfoliated from the sealing resin 7a assuming a flange structure. Further, the back surface of the semiconductor element 11 is protected by sealing resin, and hence handling of semiconductor devices during transportation becomes easy.

As mentioned above, in the present embodiment, the rigidity and reliability of packaging of the semiconductor device 100C are improved.

As has been described in the above embodiments, the present invention enables an improvement in the size of a resin layer for bonding the semiconductor element to the insulating circuit board, thereby alleviating stress which arises between the external electrodes and the module board and stress which arises between the external electrodes and the circuit board. Consequently, the reliability of packaging of the semiconductor device can be improved.

Further, the outer periphery of the semiconductor element of the semiconductor device is sealed with resin assuming a flange structure, whereby the semiconductor device assumes high rigidity. In such a semiconductor device, an improvement is made in the size of the resin layer for bonding the semiconductor element to the insulating circuit board, thereby enabling an improvement in the reliability of packaging of the semiconductor device.

Obviously many modifications and variations of the present invention are possible in the light of the above teachings. It is therefore to be understood that within the scope of the appended claims the invention may by practiced otherwise than as specifically described.

The entire disclosure of a Japanese Patent Application No. 2000-81026, filed on March 22, 2000 including specification, claims, drawings and summary, on which the Convention priority of the present application is based, are incorporated herein by reference in its entirety.

Claims

1. A semiconductor device comprising:

a semiconductor element having a primary surface and a back surface, said semiconductor element having an element electrode on the primary surface; and

a circuit board having a primary surface and a back surface, said circuit board having a board electrode on at least the back surface, said circuit board having a predetermined opening hole formed therein;

wherein the primary surface of said semiconductor element is bonded to the primary surface of said circuit board by means of an adhesive layer which is greater in size than the primary surface of said semiconductor element, and said element electrode of said semiconductor element is connected to said board electrode provided on the back surface of said circuit board via said opening hole.

2. The semiconductor device as according to claim 1, wherein the surrounding regions of the side surfaces of said semiconductor element on said circuit board are sealed with resin so as to assume a flange structure.

3. The semiconductor device as according to claim 1, wherein the surrounding regions of the side surfaces and back surface of said semiconductor element are sealed with resin.

Abstract of the Disclosure

In a semiconductor device, a semiconductor element is bonded to an insulating circuit board. A resin layer for bonding the semiconductor element to the insulating circuit board is extended so as to become greater in size than the semiconductor element. Further, the surroundings of the semiconductor element are sealed with resin. Reliability of mounting is improved by alleviating stress developing in a solder joint of the external electrodes of the circuit board.

Fig. 1

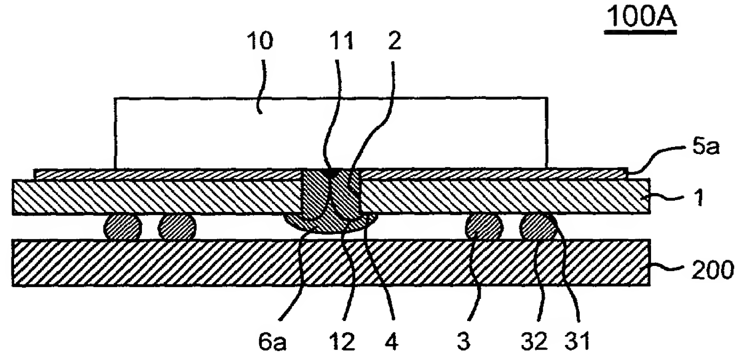


Fig. 2

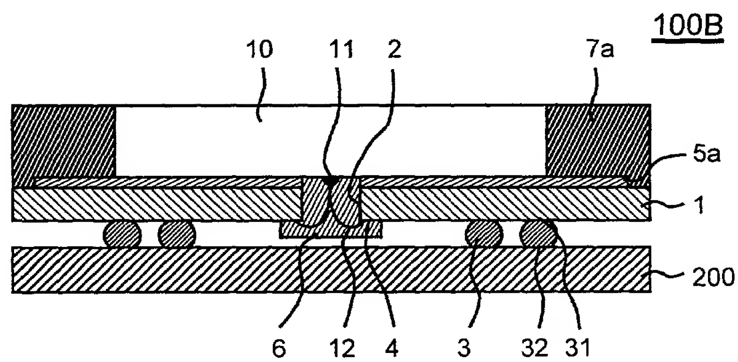


Fig. 3

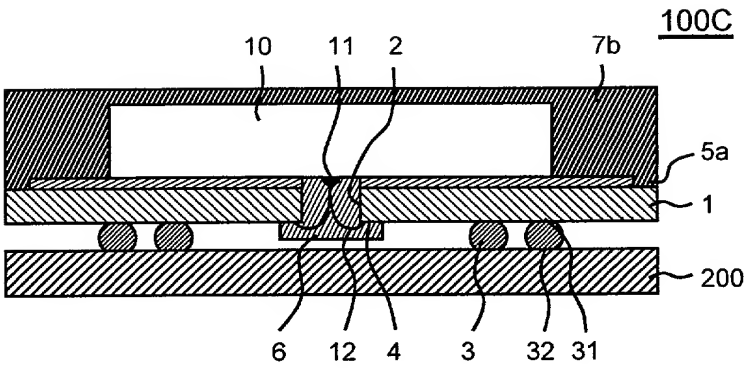


Fig. 4

Background Art

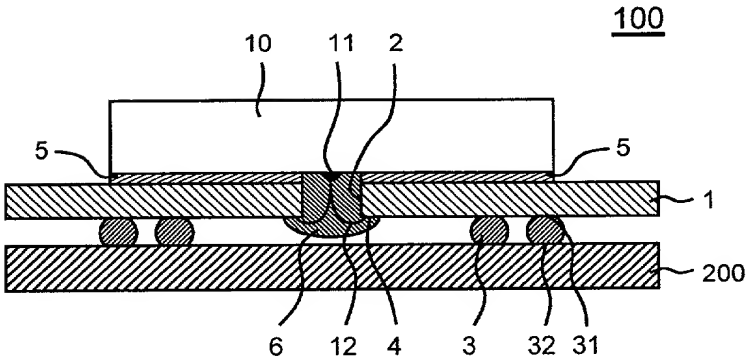
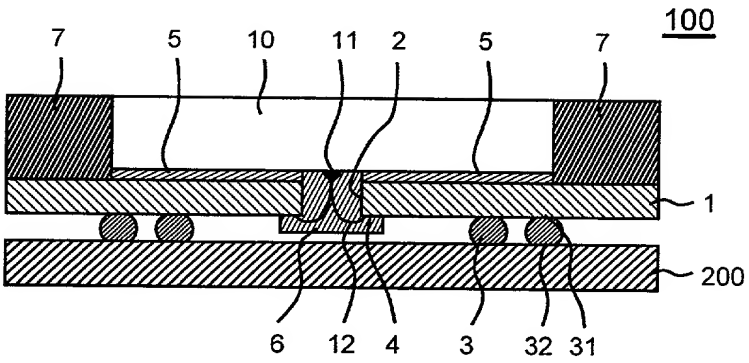


Fig. 5

Background Art



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G2705

Declaration and Power of Attorney For Patent Application
特許出願宣言書及び委任状
Japanese Language Declaration
日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者（下記の名称が複数の場合）であると信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled.

SEMICONDUCTOR DEVICE HAVING AN IMPROVED MOUNTING STRUCTURE

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ ___月___日に提出され、米国出願番号または特許協定条約国際出願番号を _____とし、
(該当する場合) _____に訂正されました。

☐ was filed on_____
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第 37 編第 1 条 56 項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第 35 編 119 条(a)-(d)項又は 365 条(b)項に基づき下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約 365 (a)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) 外国での先行出願			Priority Not Claimed 優先権主張なし
2000-081026 (Number) (番号)	Japan (Country) (国名)	22 / March / 2000 (Day/Month/Year Filed) (出願年月日)	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	☐

私は、第 35 編米国法典 119 条(e)項に基づいて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United Slates Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第 35 編 120 条に基づいて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約 365 条(c)に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第 35 編 112 条第 1 項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第 37 編 1 条 56 項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自信の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第 18 編第 1001 条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状：　私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。
(弁護士、または代理人の指名及び登録番号を明記のこと)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: (list name and registration number)

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Japanese Language Declaration

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